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Electrical and memory window properties of $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ ferroelectric gate in metal-ferroelectric-insulator-semiconductor structure

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Abstract Electrical characteristics of $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ ferroelectric films grown on HfO_2/Si wafers by sol–gel spin coating technique were investigated from the viewpoint of application as ferroelectric gates in metal-ferroelectric-insulator-semiconductor (MFIS) stacks. It was observed that the leakage current density level was 10^{-8} A/cm^2 under 14 V for moderate doping ratio. Determined memory windows from C-V characteristics of $Sr_{0.8}Bi_{2.2}Ta_2O_9$ (SBT) and $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ (x=0.04, 0.08, 0.12 and y=0.1, 0.2, 0.3) are 0.59, 0.65, 0.75, and 0.86 V at gate sweeping bias of 5 V, respectively. Some part of electronic properties of $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ with the objective to enhance memory window up to 45 % were discussed. It was interpreted that defects which are formed in Ba and Zr modified SBT affected the electronic processes like leakage current, memory window and charge trapping.

Keywords Ferroelectric · SBT · $BaZrO_3$ · Memory window; MFIS

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1 Introduction

As portable small electronic devices like mobile multi-purpose phones take a major role in communication and even data process with low power consumption, there is a confirmed increase in the demand for low scale high density nonvolatile memories. Among the various types of semiconductor memories, non-volatile ferroelectric random access memory (FeRAM) is one of the most promising due to its low power consumption and operation speed, as fast as dynamic random access memory (DRAM). The one-transistor-type (1 T-type) FeRAM, which can be formed by one ferroelectric field effect transistor (FeFET), has attracted much attention as a nonvolatile memory. It allows a non-destructive read-out, high speed, low voltage operation with high endurance, high memory density and obeys the semiconductor scaling rule. On the other hand, due to interdiffusion of constituent elements of the film and substrate during the high temperature crystallization process, fabricating a ferroelectric gate on Si with the above properties has yet to be achieved. To solve this difficulty an insulator buffer layer is inserted between the ferroelectric film and Si substrate. In fact, in metal-ferroelectric-insulator-semiconductor (MFIS) stack used in FeFETs a typical ferroelectric gate material with high remanent polarization generates a relatively large voltage drop in the insulating layer. This results in a depolarizing electric field which

neutralizes the polarization in the ferroelectric film. Consequently, the retention time is short. Additionally, the charge induced by switching the polarization of ferroelectric material is sometimes much higher than the maximum induced charge in the insulator layer. Once it exceeds the maximum value the insulating layer may breakdown before the polarization is saturated in ferroelectric gate. As a matter of fact, in order to match the charge (~1 $\mu C/cm^2$) required to control the channel conductivity in MFIS used in 1 T-type memory operation, the ferroelectric gate material needs to have a low remanent polarization (P_r). Otherwise, the majority of the voltage is applied to the dielectric layer resulting in unsaturated ferroelectric loops, short retention time and higher device operation voltage. Theoretically, a ferroelectric material with high coercive electric field shows a comparatively larger memory window [1]. So, a ferroelectric material having a low remanent polarization, high coercive field and low relative dielectric constant is desired as a gate material for FeFET type FeRAMs.

Bi-layered SBT is a good candidate to meet above ferroelectric material parameters upon certain chemical modification because it has low P_r and fatigue-free properties even with platinum electrodes. That is the reason why SBT was previously investigated as a gate on different insulators like HfO_2 [2–6], HfTaO [7, 8], HfAlO [9–11] and etc. However, remanent polarization of 10 $\mu C/cm^2$ and relative dielectric constant of 200 are still too high for 1 T-type FeRAMs.

In current work, capacitance-voltage and electronic properties of modified SBT were investigated. SBT was specifically engineered by Ba and Zr incorporation as a candidate gate material for 1 T-type memory applications. The motivation for this modification is that the origin of ferroelectricity in SBT is the off-center displacement of Ta ions in the octahedra and the rotation/tilting of TaO_6 octahedral itself. Additionally, Sr atom position in the lattice between two TaO_6 octahedrals plays a crucial role [12] in determining the ferroelectric parameters. Modification and ferroelectric details were discussed in Refs.13-15. In the present article, it is reported the some electrical properties like capacitance, memory window and leakage current of $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ films as ferroelectric gate deposited on HfO_2 in MFIS stack.

2 Experimental

MFIS stacks were fabricated as follows: initially, the HfO_2(7 nm) coated Si (p-type) wafer substrates were annealed in a rapid thermal annealing furnace (RTA) at 800°C for 1 min in O_2 atm. to produce a low leakage insulator film. Then, sol–gel solutions of SBT and $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ (0.33 mol/kg concentration Toshima MFG Co. Ltd.) were spin coated on HfO_2/Si substrate at 2500 rpm for 30 s. Later, the coated films were successively dried on hot plates at 155°C for 2 min, 240°C for 3 min and 400°C for 2 min to evaporate the solvent and remove the volatile organic compounds. After that, the films were fired in RTA furnace at 750°C for 1 min in O_2 atm. This process was repeated several times to produce 260 nm thick films. Then, the films were crystallized in a RTA furnace at 750°C in O_2 atm. for 30 min. For measurements of electrical properties circular platinum top electrodes with areas of 3.14×10^{-4} cm^2 were deposited by electron beam evaporation through a shadow mask. Finally, a backside contact of the Si substrate was formed by thermal evaporation of a layer of aluminum in order to reduce the contact resistance. Table 1 shows the sample definitions of MFIS stacks. Sample names were given respect to Ba and Zr ratio in ferroelectric gate film as follows: SBT(Ba,Zr)0 for $Sr_{0.8}Bi_{2.2}Ta_2O_9$ and SBT(Ba,Zr)5, SBT(Ba,Zr)10, and SBT(Ba,Zr)15 for $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ with (x=0.04, y=0.1), (x=0.08, y=0.2), and (x=0.12, y=0.3), respectively. The crystalline structures of the films were investigated with a multipurpose X-ray diffractometer (X`Pert-Pro MPD, Philips). The morphology of the film surface was analyzed by atomic force microscope (AFM) of Nano-Scope III by Digital Instruments. Leakage current density versus voltage (J-V) was measured by using a HP4156C precision semiconductor parameter analyzer (Agilent). Capacitance versus voltage (C-V) was measured using a LCR Meter (Toyo Corp.) at a frequency of 1 MHz, 20 mV AC level, 100 ms hold time and varying the delay time by keeping 400 mV/s sweeping speed.

3 Results and discussion

Crystal structure and the phase formation of the films were examined by x-ray diffraction (XRD). XRD patterns of SBT films with different Ba and Zr ratios deposited on HfO_2/Si substrates are presented in Fig. 1. It can be seen that all films are in single phase of polycrystalline SBT and exhibit preferred (115) orientation of relatively high diffraction intensity which indicates that crystalline films can be

Table 1 Sample definitions of Pt/$Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$/$HfO_2$/Si (MFIS) stacks

Ba and Zr amount (mol)	Sample name
x=0, y=0	SBT(Ba,Zr)0
x=0.04, y=0.1	SBT(Ba,Zr)5
x=0.08, y=0.2	SBT(Ba,Zr)10
x=0.12, y=0.3	SBT(Ba,Zr)15

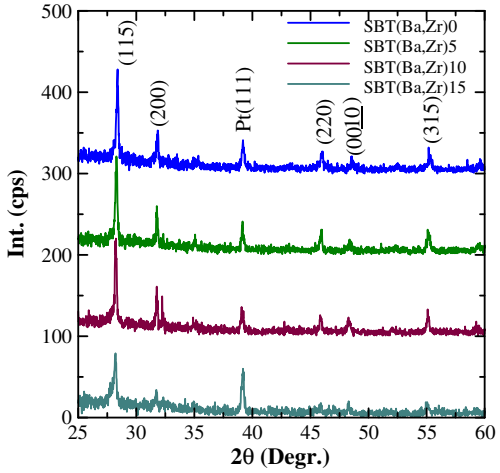

Fig. 1 XRD patterns of $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ in MFIS stack

obtained on the HfO_2 insulating buffer layer. It is noted that, for higher doping, (115) peak becomes slightly broader and less intense. This is due to a degradation of crystallinity which affects ferroelectricity by means of both lowering remanent polarization and dielectric constant [13–15].

Surface microstructure of SBT examined by SEM [15] showed that a dense structure. The well-defined facet shaped grains were formed on the surface. Figure 2 shows evaluation of the surface morphology with different Ba and Zr doping ratio measured by AFM using tapping mode. It was observed that the grain size was influenced by Ba and Zr incorporation. It was confirmed that unlike SBT the Ba and Zr incorporated films showed inhomogeneous distribution of grains with various sizes ranging from 30 nm to 300 nm. Consequently, ferroelectricity is degraded since the domain walls are inhibited in their movements as the grain size decreases. It was noted that, the root mean square (rms) value of surface roughness of SBT(Ba,Zr)15 films was 11 nm while those of the other films were 9 nm. It is known that the surface morphology has an impact on the electrical properties like leakage current. As will be discussed further in the following, it is noted that the leakage current corresponding to SBT(Ba,Zr)15 film is the highest as shown in Fig. 3.

Measured level of leakage current density in MFIS stack is crucial in memory applications. Specifically, leakage current behavior is closely related to data retention since the stored charge leaks through ferroelectric and buffer layer. As a matter of fact, higher leakage current causes less charges to be remain in ferroelectric gate film. Consequently, memory window decreases. So, the stored charge gradually decreases with time. Figure 3 presents the leakage characteristics of SBT(Ba,Zr)0, SBT(Ba,Zr)5, SBT(Ba,Zr)10, and SBT(Ba,Zr)15 MFIS diode structures at room temperature. The small peaks in the positive voltage range are attributed to the switching characteristics of ferroelectric layer. The current density versus voltage (J-V) curves reveal that the leakage current densities of SBT(Ba,Zr)0, SBT(Ba,Zr)5, and SBT(Ba,Zr)10 are on the order of 10^{-8} A/cm^2 even at an applied gate voltage of 14 V while that of SBT(Ba,Zr)15 is low 10^{-7} A/cm^2. This is attributed to higher surface roughness and doping amount. In fact, roughness leads to increased leakage current since the electric field intensity at rough surface becomes greater than that of smooth one. Moreover, increasing grain boundary regions and oxygen vacancies also degrade the insulating character as well as ferroelectric properties. It is implied that leakage current at M-F interface is enhanced [14]. Although an interface material was probably formed due to the change of chemical composition of interface, it was not determined in XRD analysis because of the low detection limit. Due to the high temperature and long annealing time, chemical composition of the film may vary. For instance, metallic bismuth may diffuse to the surface of the film or evaporate. Table 2 presents a comparison of the elemental concentration ratios of cations in pure SBT and SBT(Ba,Zr)10 solutions. To compare with the precursor solution surface and bulk compositions are measured by XPS and ICP, respectively. Residual or atmospheric carbon preferably bonds to Sr on the surface, which results in a Sr composition lower than that in the film and precursor solution. Moreover, introducing Ba and Zr increased Bi on the film surface compared to bulk. In fact, metallic Bi states are reduced by Bi-O bonding breakage and oxygen dissociation in annealing process. On the other hand, Bi might diffuse into Pt bottom electrode in capacitor structure and led to form Bi_2Pt alloy [16] via thermal annealing. Therefore, the higher the Ba and Zr doping, the more crystal defects are created. So, the trap density of the film is increased. The increasing character of leakage current density by doping is attributed to intrinsic defects, metallic Bi and microstructure. Furthermore, it is also attributed to electron trapping/detrapping. Further discussion about the leakage current was previously reported in [13–15].

Reducing the leakage current across both the ferroelectric film and the insulator layer is critically important for data retention time. Actually, a MFIS stack having high leakage current density does not neutralize the charges at an intersection of the film and insulator. Hence, the electric charges on the electrodes of the buffer layer disappear. Consequently, carriers on the Si surface disappear and the stored data can not be read out by drain current of the FeFET [17]. As a matter of fact, defects have high influence on data retention time via the mechanism of increasing leakage current as well as charge trapping/de-trapping by incorporation of Ba and Zr into crystal structure.

The capacitance versus voltage (C-V) behavior of the samples was emphasized to determine the memory window and understand the electronic characteristics of the stacks in

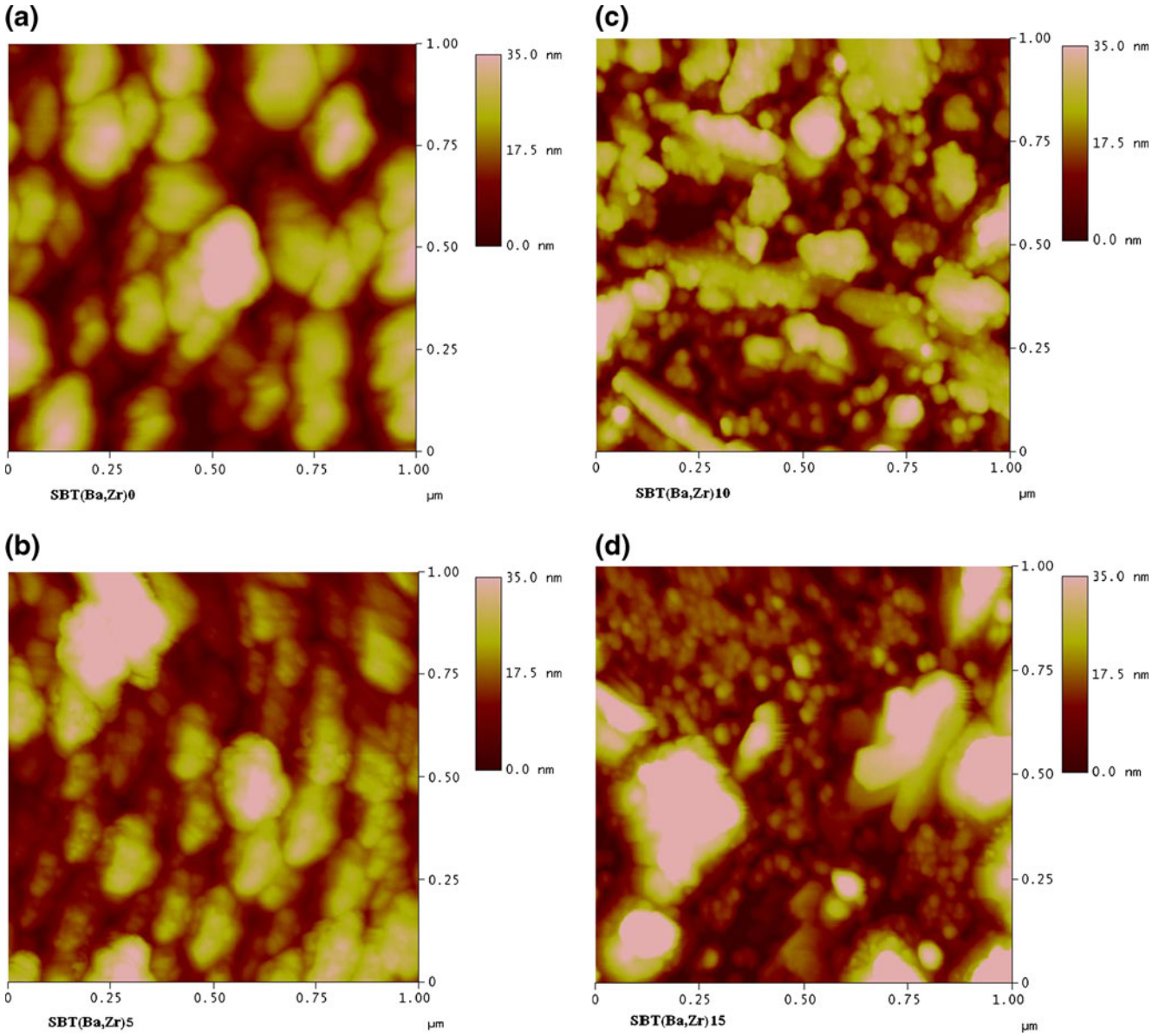

Fig. 2 Morphological studies of $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ film surfaces with different ratios: (**a**) SBT(Ba,Zr)0, (**b**) SBT(Ba,Zr)5, (**c**) SBT(Ba,Zr)10, and (**d**) SBT(Ba,Zr)15 analyzed by atomic force microscope

part. Figure 4 illustrates the C-V characteristic of MFIS structures. The bias voltage of the C-V curves was swept from negative to positive, and back to negative voltages. Basically, remanent polarization of ferroelectric gate thin film controls the surface state of Si. Due to the nature of ferroelectricity and operation of MFIS diode upon variation of applied gate voltage, C-V behavior and curve direction are dominantly influenced by polarization of ferroelectric at low voltage and trapped charge injection into the insulator buffer layer at relatively high voltages. Ferroelectric hysteretic curve due to the dipole switch induces clockwise loop and indicating the memory effect. When a negative bias is applied to the gate, the ferroelectric film has polarization and extra positive charges induce at the Si surface. An additional positive voltage is necessary to convert the Si surface from accumulation to inversion by increasing sweep voltage from negative to positive. That is the reason of shift of C-V curve toward the right. On the contrary, when the gate is positively biased and sweeps from positive to negative due to the induced extra negative charges on Si surface, additional negative voltage is needed to convert the Si surface from accumulation to inversion. So, the C-V curve is shifted toward the left side. Consequently, because of ferroelectric nature hysteresis C-V curves run clockwise direction up to a certain voltage. C-V curve width decreases since charge injection increases by increasing bias. The

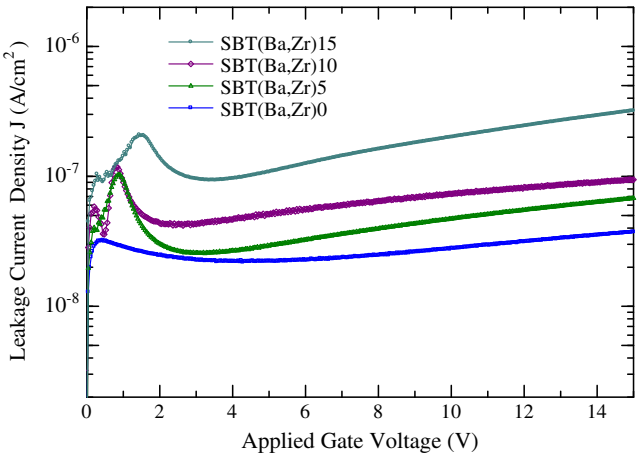

Fig. 3 Leakage current behaviors of Sr0.8-xBaxBi2.2Ta2-yZryO9/HfO2 in MFIS stack

further increase of applied voltage makes the charge injection dominant mechanism, so the C-V curve shows counterclockwise direction. As shown in Fig. 4, it appears that the capacitance changes rapidly via accumulation and inversion. This indicates that the diode has good interface properties. There is no apparent distortion in the shape of the hysteresis loop arising from applied gate voltage sweep of ±5. This indicates that the effect of interface charge traps can be neglected. On the contrary, at higher sweeping gate voltages, the hysteresis loops are degraded. This indicates that charge trapping mechanism plays a significant role. The clockwise direction of the loops arises from the ferroelectric domain reorientation [18] (switching) not from charge trapping. This means that ferroelectric hysteresis controls the Si surface potential. It is also observed that while increasing sweeping voltage, hysteresis curves are shifted to the negative voltage side. Positive charge traps like vacancies at Sr and Ba sites [19] cause this phenomenon.

The variation of flatband voltages (voltage shift of C-V curves) with the sweeping gate voltage is useful to understand memory window characteristics. Comparative characteristics of flatband voltages are plotted in Fig. 5. As increasing sweep voltage from negative to positive, flatband voltages shift to the right. On the other hand, flatband voltages shift to left side beyond a certain voltage by sweeping voltage from positive to negative. Those are the results that ferroelectric polarization delays the change in capacitance. Once again, such change in flatband at low gate voltage is due to ferroelectricity. So, the absolute difference of flatband voltages under bias voltage swept from accumulation to inversion and from inversion to accumulation is called memory window. As shown in Fig. 4 and presented in Fig. 5, flatband voltages shift to negative voltage side by increasing sweeping voltage, which indicates that positive trapped charges occur in the oxides. Above ±5 V charge injection results in decreasing the memory windows. As plotted in Fig. 6, the memory windows initially increase to maximum values with sweeping bias of 5 V due to increase in polarization. On the contrary, memory window decreases as a result of the charge injection with subsequent increase of sweeping bias above 5 V. Similarly, the memory window will be reduced as discussed in [20]. As plotted in Fig. 6, increasing the sweeping gate voltage up to ±5 V the memory windows initially increase almost symmetrically to the maximum values. This behavior reveals the ferroelectric properties. In fact, due to the increasing the sweeping gate voltage polarization increases. This is attributed to the good ferroelectric polarization switching. Increasing the gate voltage the flatband voltages shift due to increasing charge injection. In fact, increasing the sweeping gate voltage holes are injected from p-type Si substrates and trapped in HfO_2 buffer layer and ferroelectric films. Regarding SBT(Ba, Zr)0 film increasing the voltage above ±5 V charge injection severely occurs. The traps at interfaces are filled up. Hence, the polarization charges are reduced by appearing the space charges. Consequently, the memory window is drastically reduced. Compared to the other samples SBT(Ba,Zr)0 seems to have worse interface properties which is not able to prevent charge injection and trapping. On the other hand, there is a conflict since SBT(Ba,Zr)0 has the lowest level of leakage current which emphasizes the best interface properties among the samples. Currently, the exact mechanism is not clear. So, further investigation is needed for deep understanding of the relationship among the leakage current, charge injection, interface quality and trapping/detrapping of charges via increasing sweeping voltage. As can be seen in Fig. 6, the maximum memory window derived from the C-V curves are 0.59 V for SBT(Ba,Zr)0, 0.65 V for SBT(Ba,Zr)5, 0.75 V for SBT(Ba, Zr)10, and 0.86 V for SBT(Ba,Zr)15. Compared to SBT film, enhancement of memory window for Ba and Zr incorporated SBT gate-films can be elucidated by the electric field distribution between the ferroelectric film and the insulator layer. The large portion of applied voltage is disributed in modified SBT films owing to comparatively lower dielectric constant.

Table 2 Atomic concentrations

Atomic concentration (%)						
Element	Sol–gel solution		ICP (bulk)		XPS (surface)	
	SBT	SBT (Ba,Zr)10	SBT	SBT (Ba,Zr)10	SBT	SBT (Ba,Zr)10
Sr	16	14.4	16.2	15	12.8	11.1
Bi	44	44	43.4	42	43.7	45.8
Ta	40	36	40.4	37	43.5	35.6
Ba	-	1.6	-	2	-	2.0
Zr	-	4.0	-	4	-	5.5

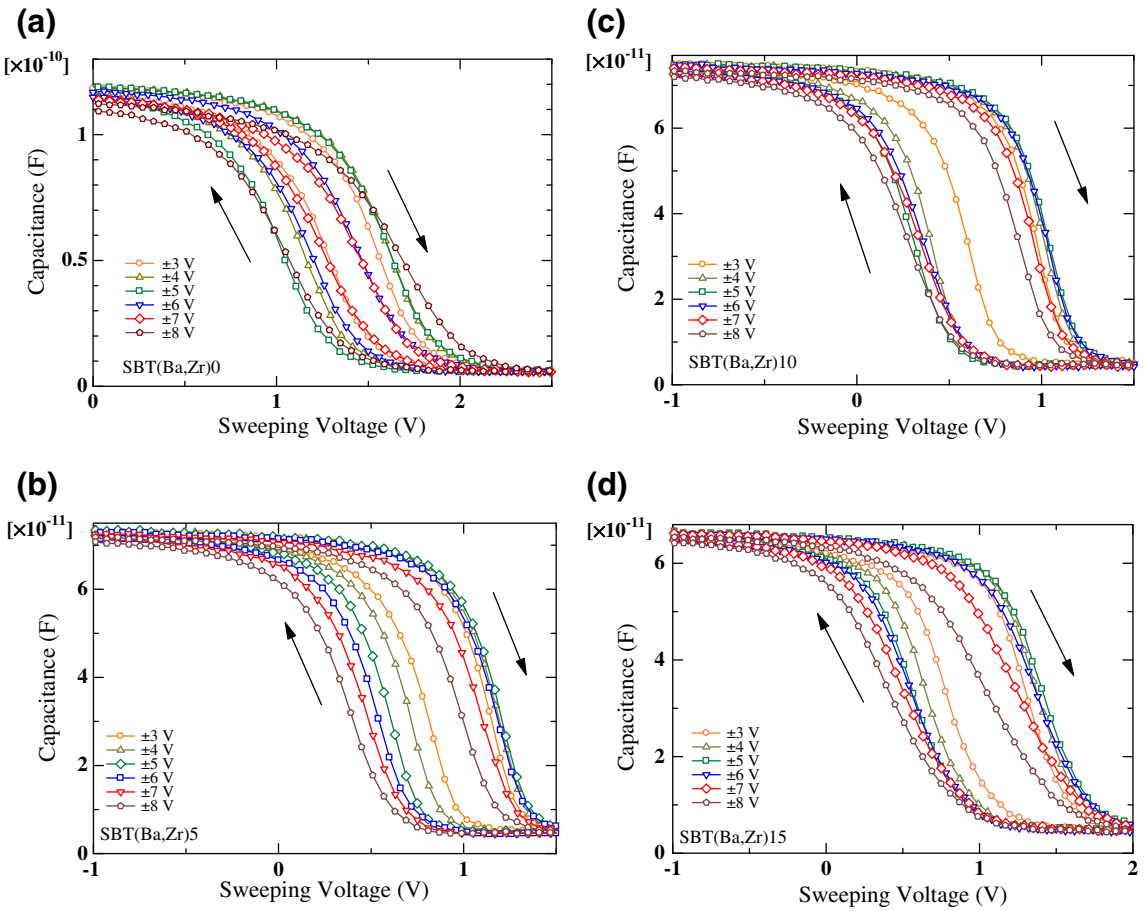

Fig. 4 Capacitance versus voltage (C-V) characteristics of $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9/HfO_2$ in MFIS stacks: (**a**) SBT(Ba,Zr)0, (**b**) SBT(Ba,Zr)5, (**c**) SBT(Ba,Zr)10, and (**d**) SBT(Ba,Zr)15 measured at 1 MHz

Owing to comparatively lower dielectric constant of modified SBT film [15], larger portion of applied voltage is distributed. Therefore, wider memory window can be obtained for SBT (Ba,Zr)5, SBT(Ba,Zr)10, and SBT(Ba,Zr)15.

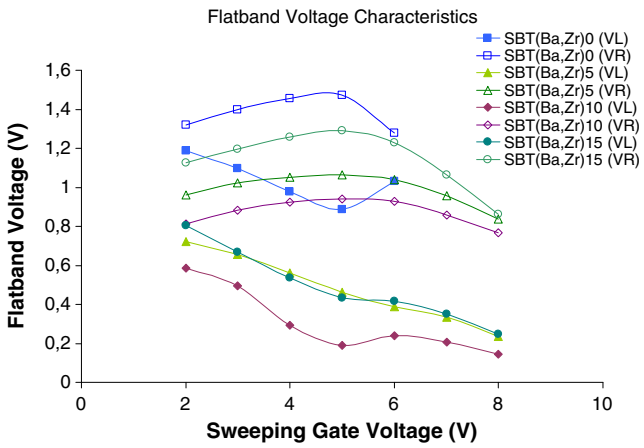

Fig. 5 Flatband voltage behavior of $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9/HfO_2$ in MFIS stacks of SBT(Ba,Zr)0, SBT(Ba,Zr)5, SBT(Ba,Zr)10, and SBT (Ba,Zr)15

Considering the dependence of memory window on thickness of both ferroelectric film and buffer layer at a particular gate voltage [21], the results above are comparable with those reported in [2–11, 17, 22, 23]. As reported in [15], it was observed that the polarization would not be saturated at the onset of charge injection, which indicated a minor hysteresis loop. So, with a low coercive field, the minor loop indicates a

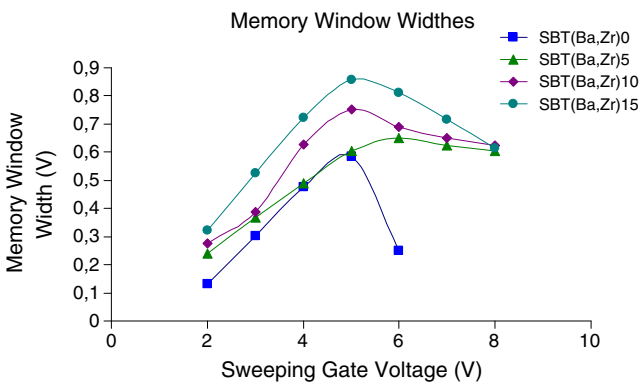

Fig. 6 Comparision of memory window widths of $Sr_{0.8-x}Ba_x Bi_{2.2}Ta_{2-y}Zr_yO_9/HfO_2$ MFIS stacks

relatively easy reversal of the domain polarization direction by the internal depolarization field. Hence, all these characteristics lead to a comparatively narrower memory window.

4 Conclusions

In conclusion, $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ films were deposited on HfO_2/Si as gate materials to fabricate MFIS stacks. Some characteristics regarding electronic properties in part, memory window widening and electrical performance in MFIS stacks were discussed by measuring capacitance and leakage current density to understand the basic properties of gate films. It was observed that $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ gate films have wider memory windows compared to SBT. Low dielectric constant of $Sr_{0.8-x}Ba_xBi_{2.2}Ta_{2-y}Zr_yO_9$ allows higher applied voltages to gate film which results in more saturated hysteresis loop. Obtaining larger memory windows for modified SBT films might lead them to apply in 1 T type memory applications upon decreasing leakage current density. So, further investigations are needed to improve material properties.

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